



# Online DRC User Guide

Updated October 2021

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## Introduction

Our website includes a design rule check (DRC), which is integrated with the online submission process. Please allow extra time during the submission process to complete the full DRC, as it takes some time to process. To begin using the DRC, navigate to the [NanoSOI Design Center](#).

## Checking the DRC through the Design Verification Tool:

Before creating an order, you can check your design using the [Design Verification Tool](#) by clicking on the left side bar.

Next, click the “Add Design to Queue” button at the top of the page. A dialog box will appear, shown below. Select the run type and the substrate type that you plan to submit for fabrication from the drop-down menus at the top of the dialog box. Next, you can choose between partial and full design rule checks. If this is the first time checking the design, please select “Partial Design Rule Check”. This will send the design through the basic checks, including calculation of the device layer exposure area and checking that features are within the allowed design area. If you are ready for the full check, select “Full Design Rule Check”.

Upload Design for Rule Checking ✕

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**Fabrication Run Type**

Multi-project Wafer Run (MPW) ✓

**Substrate Type**

Silicon: 220 nm (2 µm BOX) ✓

**Type of design check:**

**Partial Design Rule Check (DRC)**

- Device layer exposure area calculation (for cost estimation)
- Bounding box violations for device layer and metal
- Overlap check for metal and oxide openings
- Thumbnail rendering

**Full Design Rule Check (DRC)**

- All partial checks, plus space and width violations

 The full DRC can take significantly longer than the partial checks to perform. We advise starting with partial checks before proceeding to full checks.

**Other options:**

This design requires extra checks for edge-coupled devices ([what is this?](#))

Additional checks: Handling regions (Layer 202); features truncated by deep trench are indicated on DRC report

**Upload Design:**

No file chosen

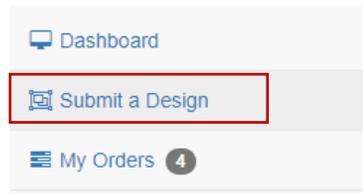
Maximum file size of 2 GB. File format must be GDSII (\*.gds) with database units of 1 nm.

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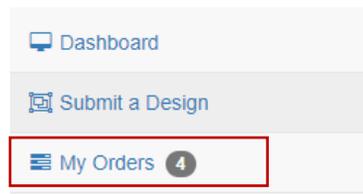
If you require edge couplers fabricated using the [deep trench process](#), please select the option for edge-coupled devices. This will ensure that the design is checked using the deep trench 8.78 x 8.78 mm design area instead of the standard 9 x 9 mm design area. Click “Choose File” and select the GDSII file you would like to check. Click the “Submit Design” button on the bottom of the dialog box to begin the design rule check. The main dialog box will close, and a second dialog box showing the progress of the design upload will appear. Once the design upload has reached 100%, please click the green “Continue” button. This will bring you back to the main design verification page. On the right side of the page, you will see a progress bar showing the progress of your design through the online DRC process. The page will automatically refresh to show the progress of the checker. Once it has completed, click the “View Report” button to show the DRC report.

## Checking the DRC through the Order Submission Process:

First, create an order using the [Submit a Design](#) page. Click “Submit a Design” on the left side bar.



Fill in the details of your order to begin the order, including uploading your design file, but do not submit the order. If the order is submitted, it can no longer be edited, and the file can no longer be modified. Once the order is created, it can be edited, and your file can be changed until you choose to submit the order. This is done through the [My Orders](#) page. Click the “My Orders” tab on the left side bar.



Once you are on the “My Orders” page, you will see the details of your order. On the right side of the page, the status of the upload, design check, and submission processes can be seen. An example is shown here:



After creating the order, the DRC results may not be visible immediately as the files can take some time to process through the system. To check if the design has passed the DRC, refresh the “My Orders” page. Once the DRC has completed, it will show the results in the “View Report” link. The icon above the link will show if the design has passed, conditionally passed, or failed. Use the “Change” link to upload a new design if revisions are required. The “Submit” check box will remain a large red “X” until you submit the design. Please submit the design once you have made all the necessary changes and you are

satisfied with the status of your design. You can submit designs that have conditionally passed, however, this indicates that you accept the risk of submitting a design containing errors.

The main difference between running the DRC from the Design Verification Tool and the “My Orders” page is the number of options that you can choose. When running the DRC from the “My Orders” page, all the DRC options are automatically selected based on your order information. Additionally, the full DRC is selected automatically instead of the partial DRC. For this reason, the DRC can take longer from the “My Orders” page compared to the Design Verification Tool.

## How to Understand the DRC Report

The DRC Report has two main parts, the Verification Report, and the Design Thumbnail. The Verification Report is at the top of the report screen. The report shows the device layer exposure area, which is useful during the design submission process for cost estimation purposes. The main results are shown in the Result and Design Violations sections. The Result shows whether the design has failed, passed, or conditionally passed. If the design has failed, revisions must be made before an order can be submitted. If the design has passed conditionally, there are some features that may not meet the design rules, such as minimum feature size and spacing. In some cases, such as tapers, these may be acceptable and so the design may still be submitted if it shows a conditional pass. When submitting a design that has passed conditionally, the user accepts the risk that the design may not turn out as drawn in the GDSII. Violations that have caused the design to fail are shown by red markers with the number of errors indicated inside the markers. Design violations that have resulted in a conditional pass are shown by the orange markers with the number of errors down inside the marker.



Exposure Area (Device Layer): 0.035 mm<sup>2</sup>

Checks Performed:

- Full Design Rule Check (DRC)

Result: **Conditional Pass**

Design Violations: **Warning** **Fail**

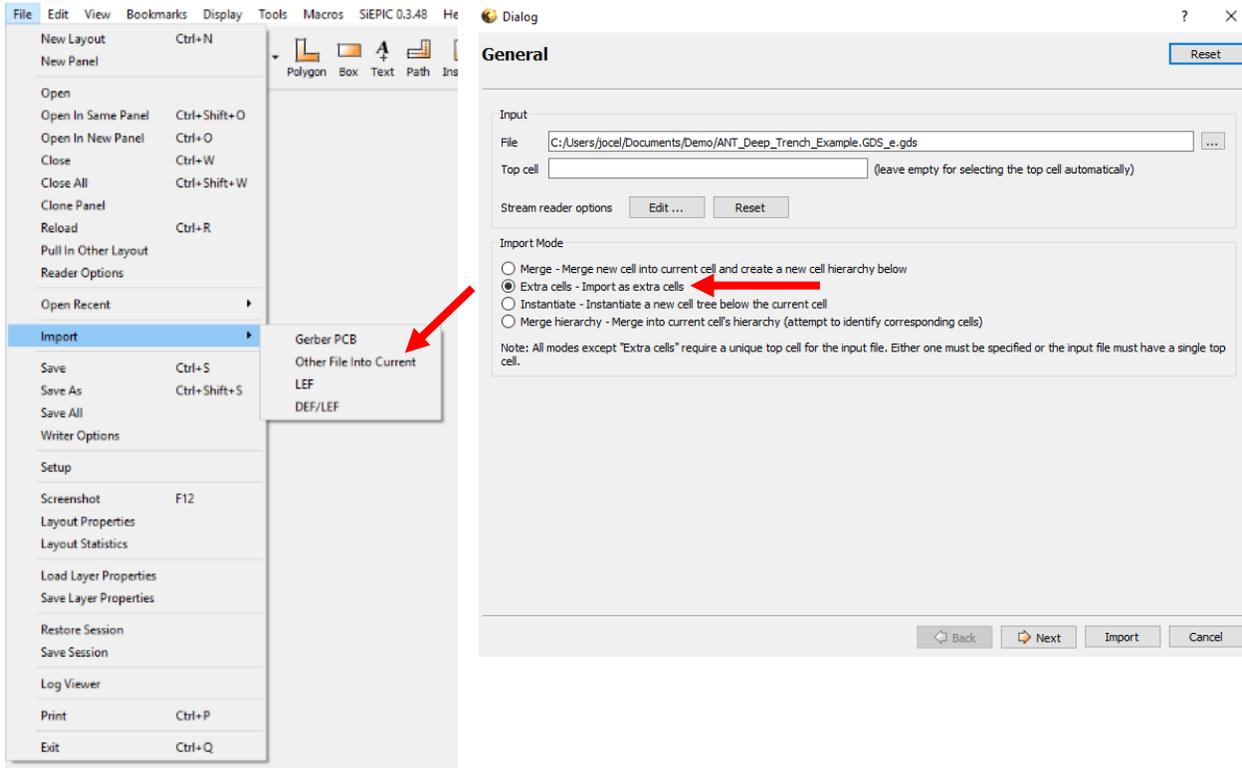
- **5** Device layer width violations (layer 301/0 on report)

[Download DRC Export](#) [Download KLayout DRC Layer Definitions](#)

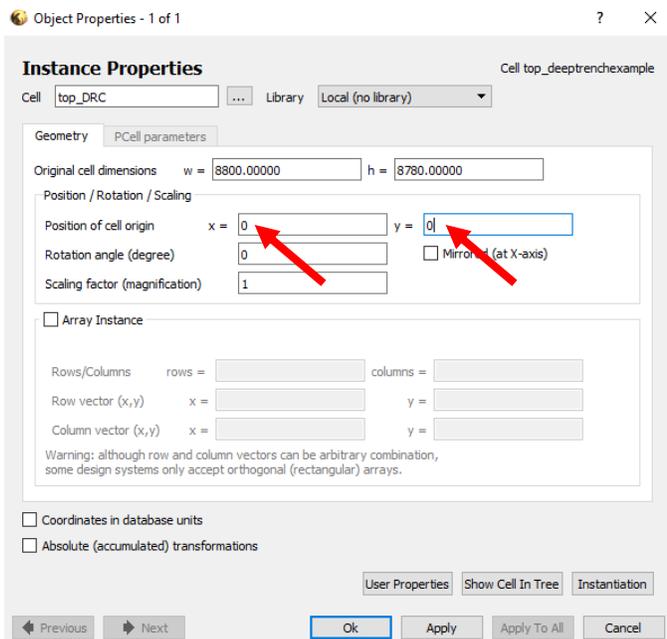
To see where in the layout the design violations occur, please click the “Download DRC Export” button. This will begin a download of a GDSII file containing the errors observed during the check. Each layer in this file corresponds to a specific error. To see what errors correspond to each layer, you can look at the online DRC report, where the layer number is listed with each error. Alternatively, you can view the error layers in KLayout by downloading the DRC Layer Definitions file. This file can be downloaded by clicking the button next to the GDSII download button.

There are two ways to look at the error file in KLayout. You can either look at the error file by itself, which is useful for seeing larger errors such as centering violations. For smaller features, such as width or spacing violations, it is difficult to see which features on the layout have caused the error. To overcome this issue, import the DRC results into your existing layout and overlay them. This will allow you to see where the design violations have occurred. To do this, open your existing design in KLayout.

To import the error file, go to File -> Import -> Other File Into Current. A dialog box will appear. Click the “...” button to select the GDSII error file. Click the “Extra Cells” radio button to import the GDSII as its own cell into KLayout. Finally, click the “Import” button on the bottom of the dialog box. This will import the GDSII error file into the existing layout.



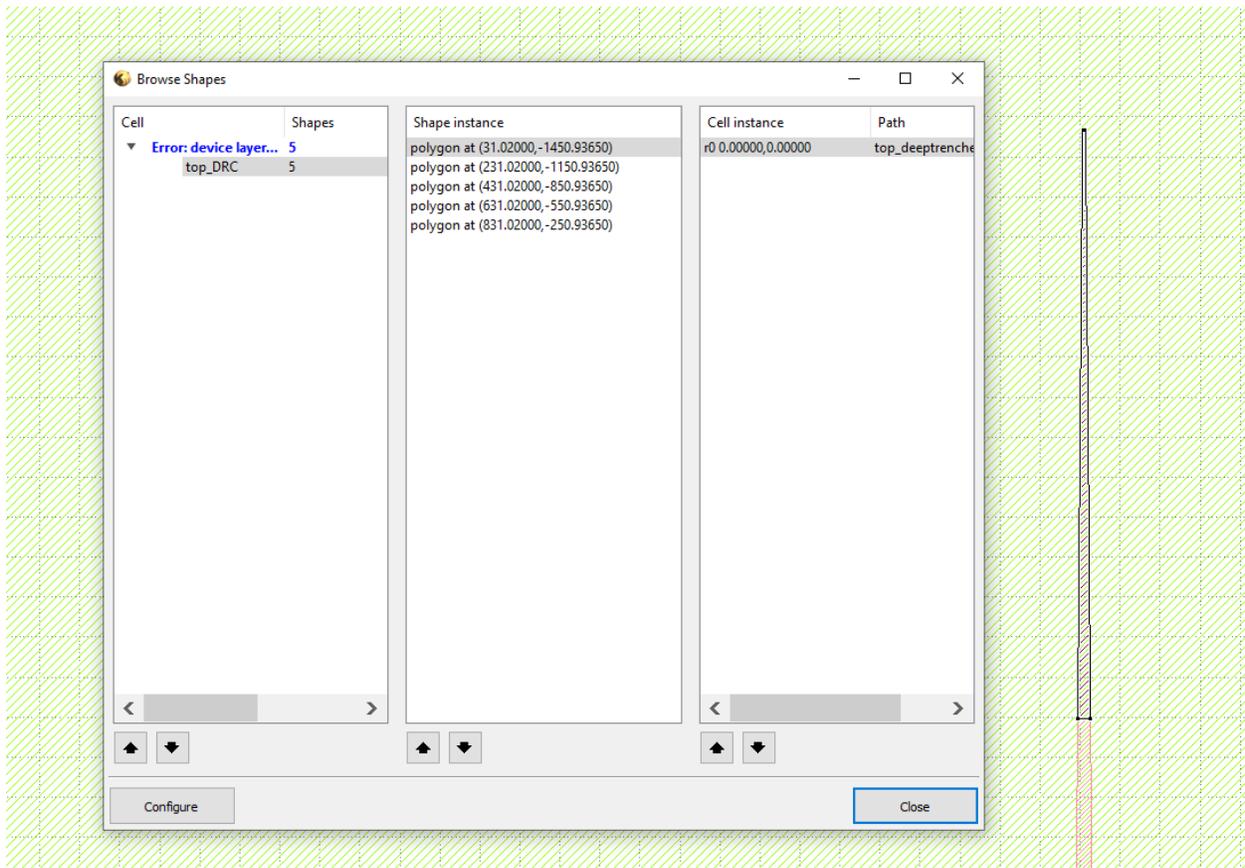
To overlay the two designs, choose the top cell of your existing design to be the current top cell. Then, highlight the cell called “top\_DRC” in the left menu in KLayout and drag it into the top cell of your original layout. To open the properties of the DRC cell, highlight the cell and click “q”, or double click the DRC cell. Set the origin to “x=0” and “y=0” and click “Okay”. The DRC error cell will now be placed correctly relative to the original layout.



The layer definitions are visible automatically if the NanoSOI PDK is active. If the NanoSOI PDK is not in use, then the layer definitions can be added manually by downloading the layer definitions file from the Verification Report. To see the layer definitions within KLayout, go to File ->Load Layer Properties. Find “NanoSOI\_Layers.lyp” downloaded from [the NanoSOI website](#) and click “Open”. This will load the layer definitions with a description of each layer on the right sidebar in KLayout as shown in the image below.



To see the errors generated by the online DRC tool on each layer, select the layer of interest on the right sidebar in KLayout, and then go to “Tools”. Select “Browse Shapes” and a separate window will appear with the error polygons listed. Use the up and down arrows to toggle through the error polygons to see exactly where each error occurs on the layout. Some errors may be acceptable; for example, the error seen in the image below is a silicon taper with dimensions smaller than 70 nm. However, the exact dimensions of this fabricated structure are not critical for this application as the taper is simply meant to dissipate the light in the waveguide. In this case, the error is acceptable because the device will function as intended even if it not fabricated exactly as shown in the GDSII. An example of an unacceptable error would be a coupling gap between a racetrack resonator and the bus waveguide that is less than the minimum spacing of 70 nm. In this case, the device would not function as expected because the devices would be merged during the fabrication process, and so this error must be corrected before submission.



The second part of the verification report page is the design thumbnail. By scrolling down to the bottom of the verification report, you can see a thumbnail of your design that has been generated by the design check. A legend describing the colour-coding of the thumbnail is located at the top of the design thumbnail page. For example, red features on the thumbnail correspond to device layer features on your design. Please view this thumbnail to ensure that your design has uploaded as expected. You may need to scroll down to view the full extents of your design.

## Technical Support

If you have technical issues or questions about the online DRC tool, please contact us at [support@appliednt.com](mailto:support@appliednt.com).